Features

- Class 2 and 3 (up to 10 meter range) compliant with Bluetooth Specification 1.1
- Fully integrated single-chip transceiver with on-chip PLL, VCO, LNA, up/down converter, and digital GFSK modem
- Seamless interface to BlueRF RXMODE2 with unidirectional / JTAG serial interface or bidirectional / DBUS serial interface
- Up to -90dBm receiver sensitivity
- Superior adjacent channel selectivity of -6 at 1MHz offset
- Support dual reference clock frequency: 13/16MHz
- Bluetooth BQB QPL qualified - ID = B00992

Application

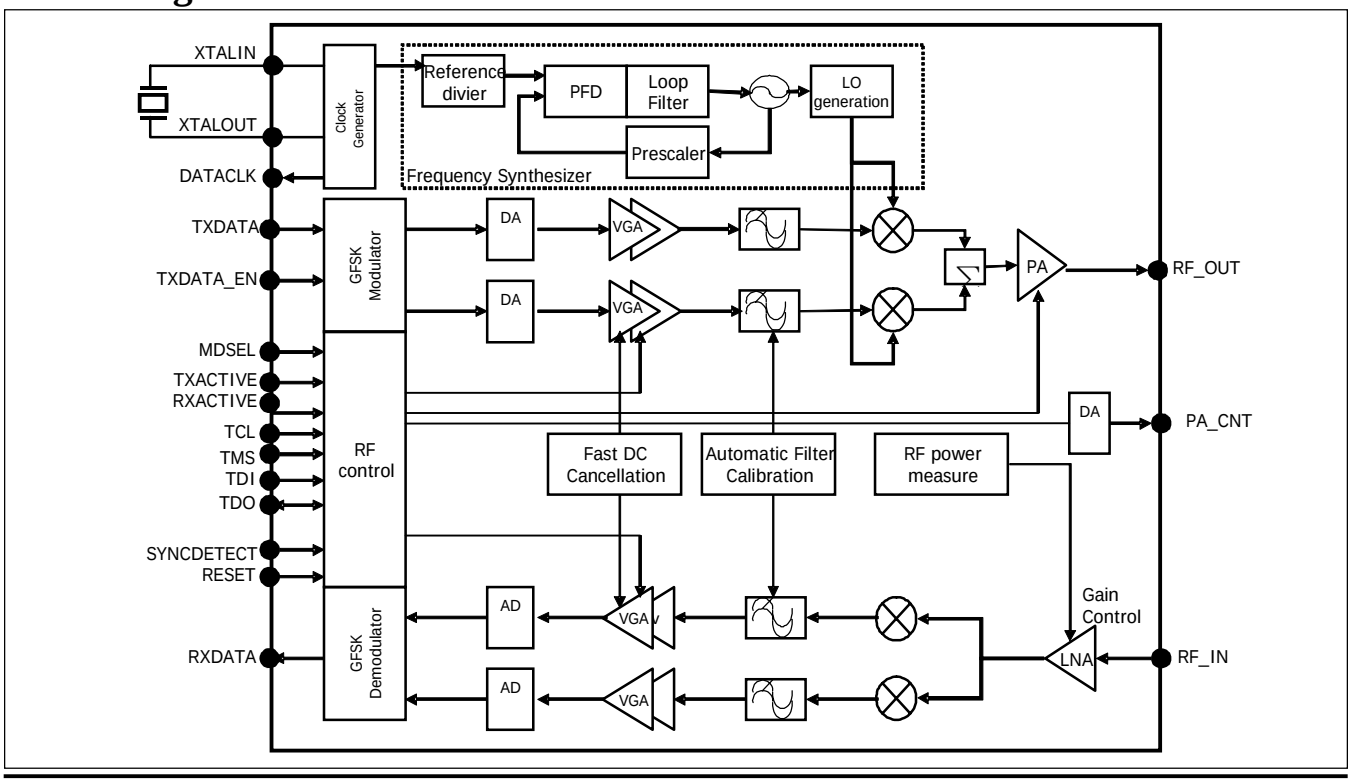
- ISM 2.4GHz wireless systems
- Mobile phones and Handset

General Descriptions

The PT8R1002 is a part of the PTI Bluetooth product family. It is a short-range microwave-frequency radio transceiver for Bluetooth links that operates in the 2.4 GHz to 2.5 GHz ISM band. The device consists of a fully integrated 2.4 GHz radio transceiver with GFSK modem. This radio IC is based on PTI's proprietary radio architecture employing direct conversion scheme, which offers superior channel selectivity, and is implemented in CMOS technology, which provides low cost integrated RF and baseband solutions for Bluetooth applications.

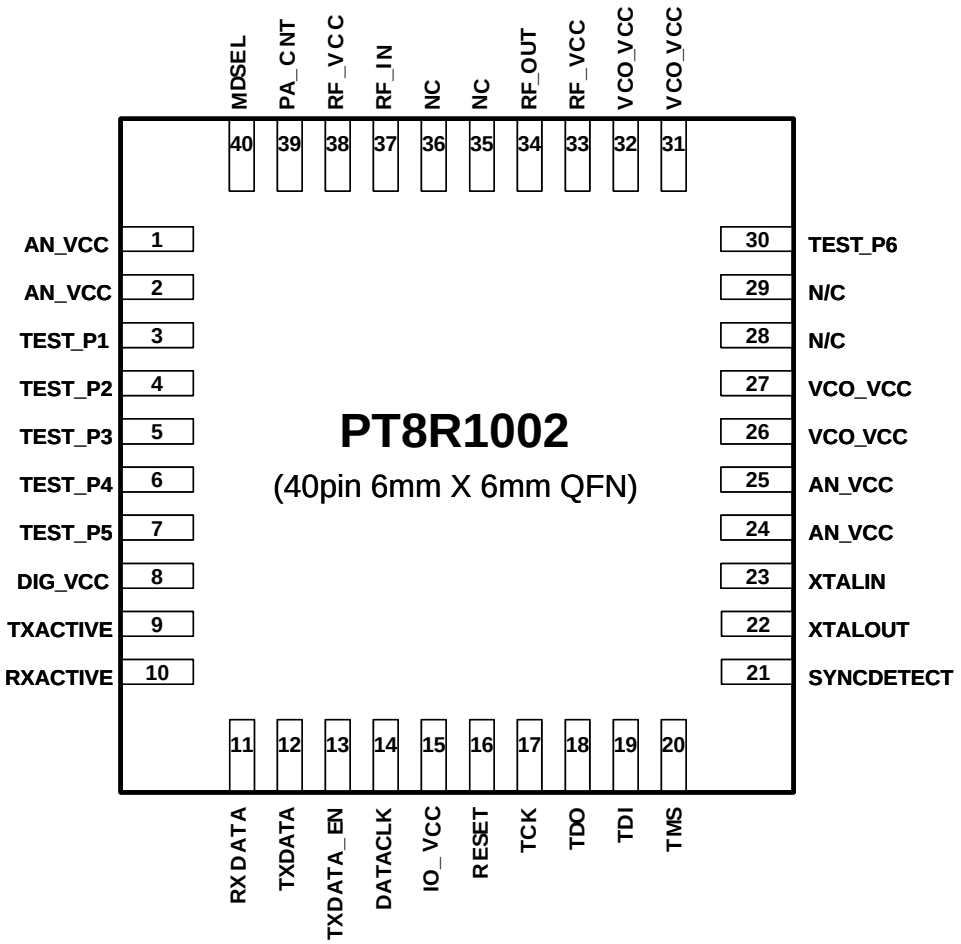
The PT8R1002 incorporates the complete receive and transmit components including PLL, VCO, LNA, up/down converter, channel select filters, and digital GFSK modem.

Block Diagram



Pin Information

Pin Configuration



Ordering Information

Device	Components	Packing	Part Number Representation		
			Lot Traveler	Label	Marking
QFN40	Normal	Tray	PT8R1002ZB	PT8R1002ZB	PT8R1002ZB
		T&R	PT8R1002ZBX	PT8R1002ZBX	PT8R1002ZB
	Pb(Lead) Free	Tray	PT8R1002ZBE	PT8R1002ZBE	PT8R1002ZBE
		T&R	PT8R1002ZBXE	PT8R1002ZBXE	PT8R1002ZBE

Pin Description

Pin No	Pin Name	Type	Description
1, 2, 24, 25	AN_VCC	Power	Power supply for analog baseband core (2.7V)
3, 4	TEST_P1, TEST_P2	DO/AO	serial data, test purpose only (see note3)
5, 6, 7	TEST_P3 - TEST_P5	DO	serial data, test purpose only (see note3)
8	DIG_VCC	Power	supply for digital core (2.7V)
9	TXACTIVE	DI	transmitter enable, active high
10	RXACTIVE	DI	receiver enable, active high
11	RXDATA	DO	serial data, receive data
12	TXDATA	DB	serial data, transmit data
13	TXDATA_EN	DI	active high, timing reference of valid data
14	DATACLK	DO	clock, 13/16MHz reference data clock
15	IO_VCC	Power	supply for digital I/O (3.3V)
16	RESET	DI	active low, reset signal for internal registers
17	TCK	DI	clock, a serial register interface clock
18	TDO	DB	serial data, Phy control register serial data output
19	TDI	DI	serial data, Phy control register serial data input
20	TMS	DI	serial data, control signal of Phy's TAP controller
21	SYNCDETECT	DI	active high, indication of SYNC word detection
22	XTALOUT	AO	clock, reference crystal output (see note2)
23	XTALIN	AI	clock, reference crystal input (see note2)
26, 27, 31, 32	VCO_VCC	Power	supply for PLL block (2.7V)
28, 29, 35, 36	NC	-	No connection
30	TEST_P6	AO	analog, test purpose only (see note3)
33, 38	RF_VCC	Power	supply for RF block (2.7V)
34	RF_OUT	AO	analog, 2.4GHz transmitted signal from internal PA
37	RF_IN	AI	analog, 2.4GHz received signal from antenna
39	PA_CNT	AO	analog, power control to external power amplifier
40	MDSEL	DI	select data, BlueRF™ directional mode selection pin (see note1)

Note : 1. The pin indicates the directional mode of BlueRF™ RXMODE2.

Pin Name	I/O	Type	BlueRF™ RXMODE2 BlueRF RXMODE2	Bidirectional interface Unidirectional interface
MDSEL	DI	select data	LOW	HIGH
TXACTIVE	DI	active high	Don' t use	BTXEN
RXACTIVE	DI	active high	Don' t use	BRXEN
TXDATA_EN	DI	active high	Don' t use	BPAEN
TXDATA	DB	serial data	BTXD Transmit (DI), Receiver (DO)	 BTXD (DI)
RXDATA	DO	serial data	Don' t use	BRXD
SYNCDETECT	DI	active high	BPKTCTL	BPKTCTL
DATACLK	DO	clock	BRCLK	BRCLK
RESET	DI	active low	BnPWR	BnPWR
TCK	DI	SPI clock	BDCLK	BDCLK
TMS	DI	control data	BnDEN	BnDEN
TDI	DI	serial data	Don' t use	BMISO
TDO	DB	serial data	BDDATA Write (DI), Read (DO)	BMOSI (DO)

2. The default supporting reference clock is 13MHz. To use 16MHz as reference clock, it is necessary to program the RF register through serial interface at the initial stage. The register description should be referred for the change.
3. These pins should be open in normal operation.

Functional Description

Bluetooth is an open specification for short-range data communications. It operates in the globally available 2.4 GHz to 2.5 GHz ISM free band and uses fast frequency hopping (1600 hop/s) over 79 available channels (2.402 to 2.480 GHz) with a maximum data rate of 1 Mbit/s.

The PT8R1002 is intended for the use in 2.4GHz ISM frequency band wireless systems, especially, Bluetooth. The transceiver consists of a fully integrated 2.4 GHz radio transceiver, frequency-hopping synthesizer, and analog-to-digital and digital-to-analog converters for the baseband interface. As illustrated in Figure 1, the radio module requires only an external antenna, antenna switch and crystal to complete the analog front end.

RF receiver

The receiver front-end converts the incoming RF signal in 2.4GHz ISM frequency band to a digitized signal for digital signal processing. The receiver is composed of a LNA, a complex RF-to-Baseband down conversion Mixer, an AGC/complex filter, a dual ADC for the I/Q signal paths, and phase locked loop synthesized local oscillator. The first stage is a single-ended LNA with external matching circuit. The LNA is followed by quadrature down conversion mixers. The down conversion mixer employs PTI' s proprietary technologies to minimize RF coupling and DC offsets.

Channel selection filter and AGC

With the use of direct down-conversion scheme, the complex baseband filters carry out excellent channel selection and image-free operations. As a result, the receiver exceeds the Bluetooth 1.1 requirements for adjacent channel & image rejection and provides superior performances in the presence of ISM-band RF interferers.

The AGC and filter are optimally designed to meet both the stringent requirements of gain setting and Adjacent Channel Selectivity (ACS) in Bluetooth. In ISM frequency band applications, excellent adjacent channel selectivity is required, because there can be too many blockers operating simultaneously. Thus, both channel filter and AGC circuits must have high linearity and low noise performance. The first channel filter and first AGC used have IIP3 greater than 30dBm. The remaining channel filters and AGC' s are optimized to obtain high ACS.

RF transmitter

The transmitter is composed of a dual DAC for the I/Q signal paths, channel filter, Baseband-to-RF up- conversion Mixer, and power amplifier with 2 dBm output power. The phase locked loop frequency synthesizer is shared with RF receiver to minimize the hardware components. The transmitter features a direct up-conversion scheme to minimize the frequency drift during a transmit timeslot and also results in a well-controlled modulation index. The baseband channel filter offers excellent out-of-band suppression and equalized signals to minimize the interference with the on-chip receiver. With the nominal transmit power of 0 dBm, the transmitter can be used in class 2 and class 3 radios, and can be simply implemented in class 1 with an external RF power amplifier.

PLL

The radio synthesizer is fully integrated and thus does not require any external elements. It is designed with PTI' s proprietary frequency synthesizer technologies, which minimize phase noise and coupling to the RF amplifiers. An on-chip reference oscillator is provided and requires an external crystal or a reference clock. The external crystal (reference clock) frequency should be 13MHz or 16MHz with 20 ppm accuracy.

Baseband modem

The baseband GFSK modem is implemented in a compact dedicated logic that provides excellent performance in the presence of noise, interferers, and frequency offset/drift, while consuming very small power. The baseband modem interface is designed to transfer Bluetooth data between PT8R1002 and a baseband controller. The GFSK demodulator performs frequency demodulation. The inherent frequency offset compensation block can guarantee stable operation in the present of large frequency deviation, which is activated with SYNCDETECT asserted. The GFSK modulator provides a precise modulation index control and a Gaussian spectral shaping.

PT8R1002 supports the BlueRF™ RXMODE2 Bluetooth interface with both unidirectional and JTAG serial interface or bidirectional and DBUS serial interface which are all compatible with the PTI PT8R1202 Bluetooth Baseband controller. In this mode, external Bluetooth baseband delivers the SYNCWORD detection indication to PT8R1002 when it detects a Bluetooth SYNCWORD in received data.

I/O Description

RF interface

The radio interface establishes the connection of antenna-to-LNA in receiving mode and antenna-to-power amplifier in transmitting mode. The actual configuration of RF front-end can be seen Figure 1. An antenna filter is located between the antenna and SPDT (Single Pole Double Throw) switch. The antenna filter blocks unwanted signals in receive mode and suppresses harmonics in the transmit mode. The filter can be either a discrete component or fully integrated in ceramic substrate. The SPDT switch isolates the transmit path and the receive path and thus impedance can be matched for entire signal path. A matching circuit is placed between LNA_IN pin and SPDT switch to match the 50 ohm source to the complex input impedance of the LNA. Another external matching circuit is required at PA_OUT to transfer maximum power to the antenna.

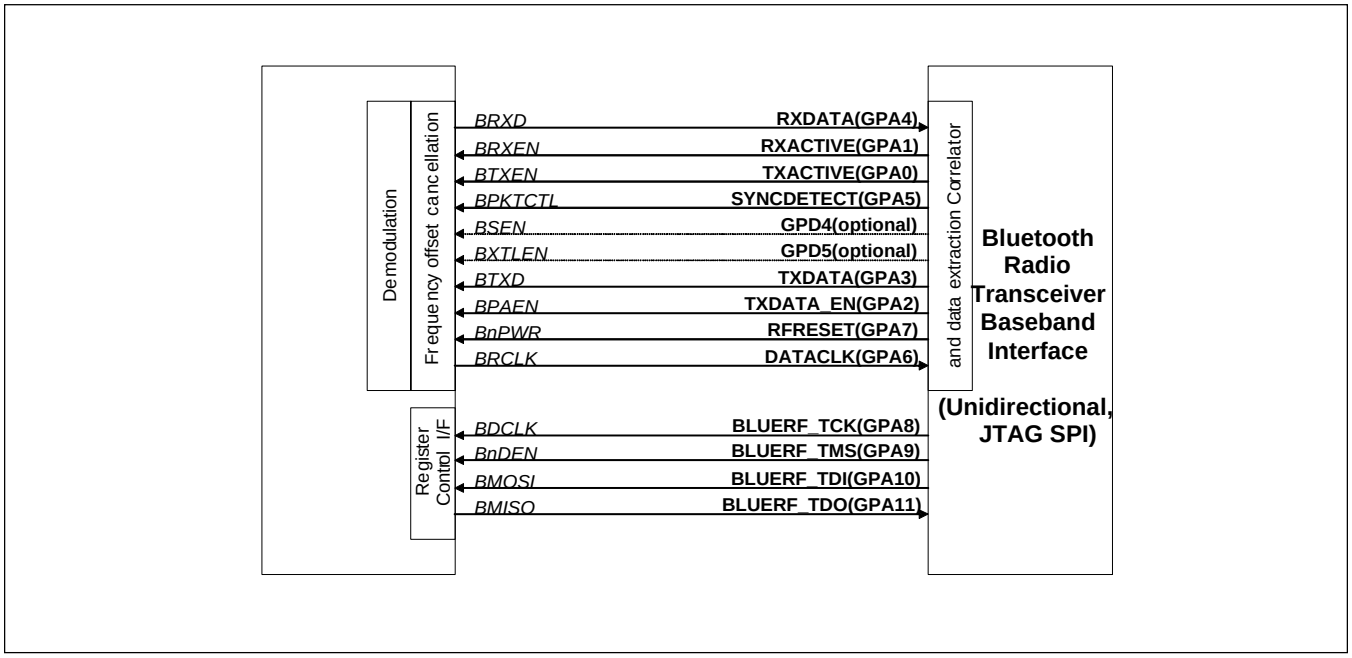
BlueRF RXMODE2 baseband interface

PT8R1002 supports the BlueRF™ RXMODE2 Bluetooth radio interface with unidirectional and JTAG serial programming interfaces or bidirectional and DBUS serial programming interface, which are compatible with the PTI PT12002 Bluetooth baseband controller. In RXMODE2, the SYNCWORD correlator is located in baseband controller, and it detects signal feeds into PT8R1002.

Unidirectional interface

The interface connections for unidirectional mode are shown in Figure 4.

Figure 4. BlueRF RXMOD2 Unidirectional baseband interface



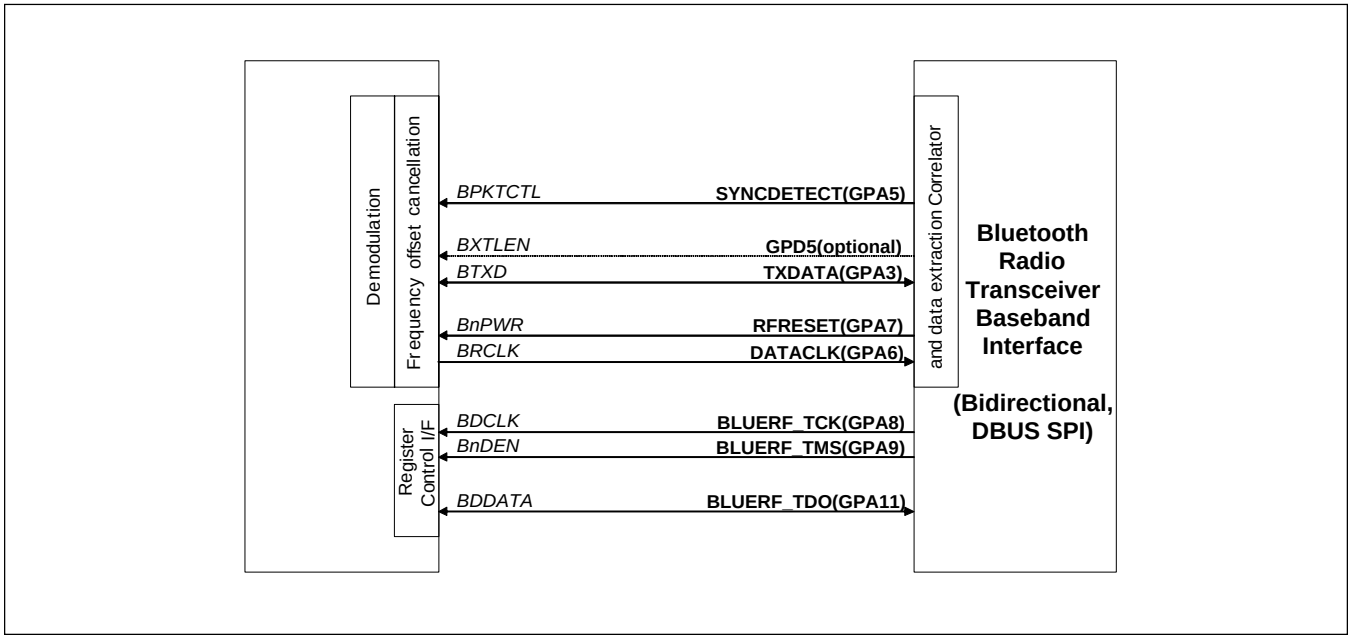
The unidirectional mode allows the PT8R1002 to be controlled with minimum reference to the previous state of the interface. This allows the state of PT8R1002 to be inferred by examining the logic levels on the interface signals. The unidirectional interface can be split into two subsections: RF data and control path, register control interface. In BlueRF interface, ten signals are used in the RF data and control path, and four in the register control interface. All of the signals are unidirectional. However, the BSEN (Hop frequency synthesizer enable) and BXTLEN (a strobe which enables the RF oscillator) are not supported as explicit signal in the PT8R1002. Instead, these equivalents functions can be supported using serial programming through JTAG interface. The unidirectional interface requires that the PT8R1002 control registers interface to the Baseband via an IEEE 1149.1 JTAG interface. The unidirectional interface requires that the Baseband portion of the interface is referenced to a Baseband generated clock.

Bidirectional interface

The bidirectional mode provides the lowest pin count interface between the baseband and RF piece. The interface connections for bidirectional mode are shown as follows:

As similar to unidirectional interface, the bidirectional interface can be split into two subsections: RF data and control path, register control interface. The bidirectional interface uses a DBus control register interface. In BlueRF interface, five signals are used in the RF data and control path, and three in the register control interface. There are two bidirectional signals such as BTXD and BDDATA. The direction of the two bidirectional pads (BTXD, BDDATA) is controlled by separate state machine in the baseband and PT8R1002. The baseband state machine is the master and controls the state machine in the PT8R1002 in an open loop manner. To prevent bidirectional data contention, baseband must ensure not to occur during reset and normal operation.

Figure 5. BlueRF RXMOD2 Bidirectional baseband interface



Transmit operation in Unidirectional interface

The primary signal for data transmit is TXACTIVE signal. The actual data transmission starts after TXDATA_EN provided by baseband. During transmit mode, DATACLK is sent from PT8R1002 to baseband as a timing reference. The baseband circuit transmits data to the PT8R1002 at the falling edge of DATACLK, whereas the PT8R1002 latches the data at the rising edge of DATACLK. The state of PT8R1002 transitions from the ***idle state*** when the baseband drives TXACTIVE *HIGH*. TXACTIVE enables all the transmit circuitry except for the final output stage. TXACTIVE is driven high at a time $T_{TuningTX}$ before the hop frequency synthesizer has settled to allow any frequency offsets caused by the TX circuitry to be eliminated. Either when, or just before, the TX circuitry has correctly settled on frequency, the baseband drives TXDATA_EN *HIGH*, which enables the PA stage, and causes the unidirectional interface to enter the ***transmit data state***. The baseband drives data to the PT8R1002 on the falling edge of DATACLK, and the PT8R1002 reads the transmit data on the rising edge. When all the data has been transmitted, the baseband drives TXDATA_EN and TXACTIVE *LOW* to disable the PA stage and return to the ***idle state***.

Figure 6. Transmit procedure timing diagram in unidirectional interface

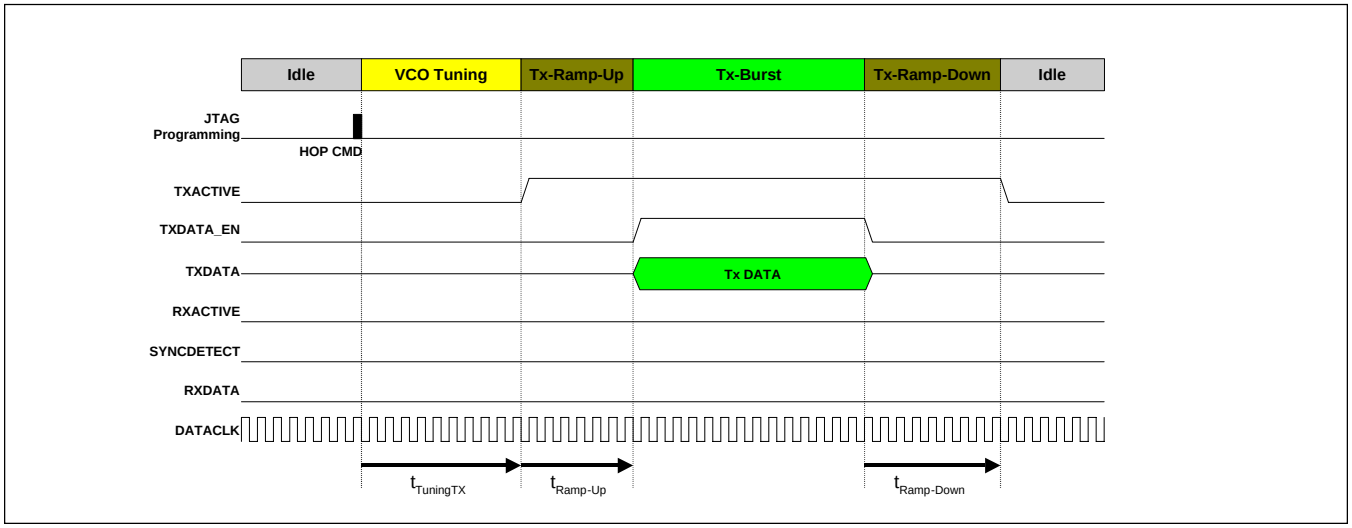
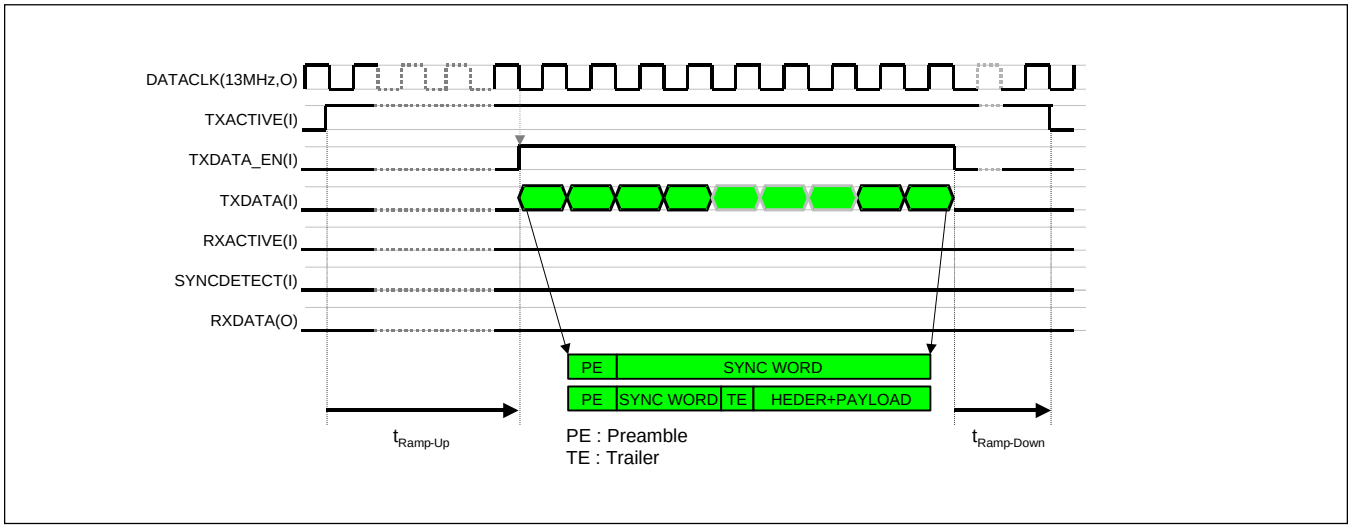


Figure 7. Transmit signal timing diagram in unidirectional interface



Transmit operation in Bidirectional interface

Unlike unidirectional interface, the primary procedure for data transmit is to activate internal TXACTIVE signal by writing *HIGH* to TXA field of BT_RF_PLL_CTRL1 through DBUS interface. The actual transmission starts after *HIGH* value of SYNCDETECT provided by baseband. During transmit mode, DATACLK is sent from PT8R1002 to baseband as a timing reference. The baseband circuit transmits data to the PT8R1002 at the falling edge of DATACLK, where the PT8R1002 latches the data at the rising edge of DATACLK. The PT8R1002 transitions from the ***idle state*** when the baseband writes *HIGH* to TXA field of BT_RF_PLL_CTRL1 through DBUS interface. Updating *HIGH* to that field enables all the transmit circuitry except for the final output stage. DBUS writing is executed at a time $T_{TuningTX}$ before the hop frequency synthesizer has settled to allow any frequency offsets caused by the TX circuitry to be eliminated. Either when, or just before, the TX circuitry has correctly settled on frequency, the baseband drives SYNCDETCT *HIGH*, which enables the PA stage, and causes the bidirectional interface to enter the ***transmit data state***. The baseband drives data to the PT8R1002 on the falling edge of DATACLK, and the PT8R1002 reads the transmit data on the rising edge. When all the data has been transmitted, baseband should write *LOW* to TXA field of BT_RF_PLL_CTRL1 to disable the PA stage and return to the ***idle state***.

Figure 8. Transmit signal timing diagram in bidirectional interface

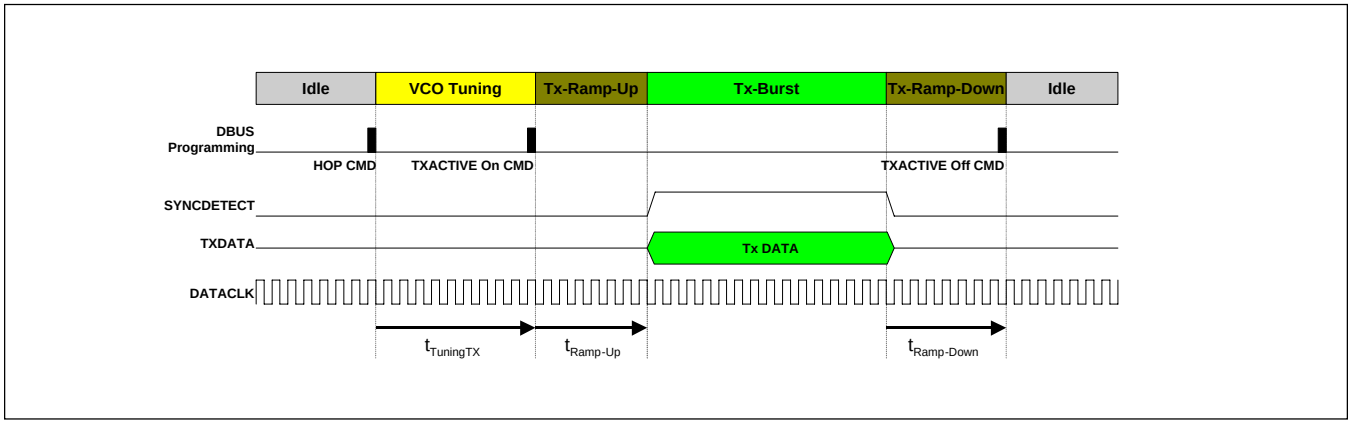
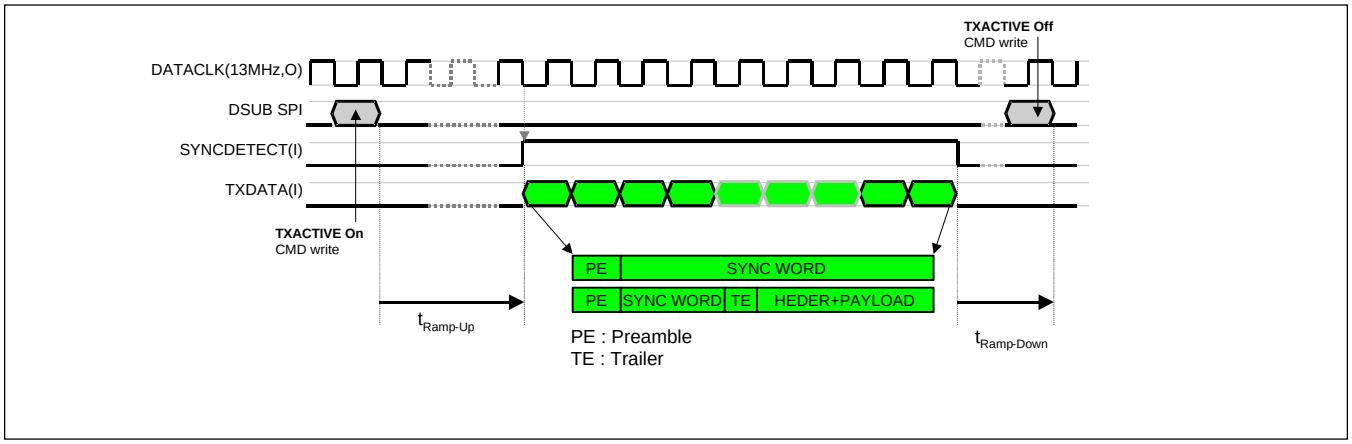


Figure 9. Transmit signal timing diagram in bidirectional interface



Receive operation in Unidirectional interface

The primary signal for data reception is RXACTIVE signal. When RXACTIVE goes to high, the RF circuitry starts to operate and send data after fixed time from RXACTIVE. The baseband receives data and searches for the access code. During receive mode, DATACLK is sent from PT8R1002 to baseband as a timing reference. The PT8R1002 circuit sends the data to baseband at the rising edge of DATACLK, where the baseband latches the data at the falling edge of DATACLK. Prior to receiving information over air, the baseband transfers control information including the hop frequency over the JTAG interfaces, and enters PT8R1002 into ***search access code state*** after fixed time to turn on receiver circuitry by driving RXACTIVE *HIGH*. In the ***search access code state***, the baseband performs all of the tasks required to correlate with the access code from the receive data. When the baseband has correlated the access code, then it drives SYNCDETECT *HIGH* and makes PT8R1002 enter into ***receive payload state***. During the payload, PT8R1002 eliminates any frequency offset between local and remote Bluetooth devices based on its measurement during syncword acquisition. PT8R1002 transmits demodulated data to the baseband at half frequency of DATACLK, which can be read by the baseband using appropriate timing recovery algorithm. The unidirectional interface is returns to the ***idle state*** with the baseband driving RXACTIVE *LOW* after a fixed interval of T_{RxOff}.

Figure 10. Receiver procedure timing-diagram in unidirectional interface

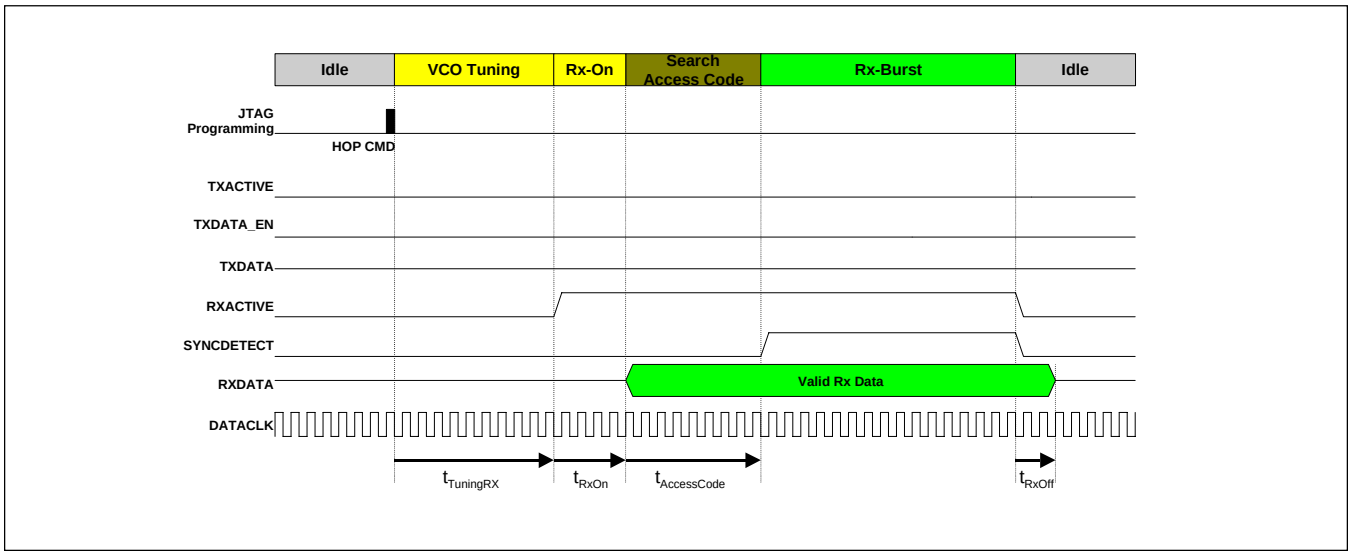
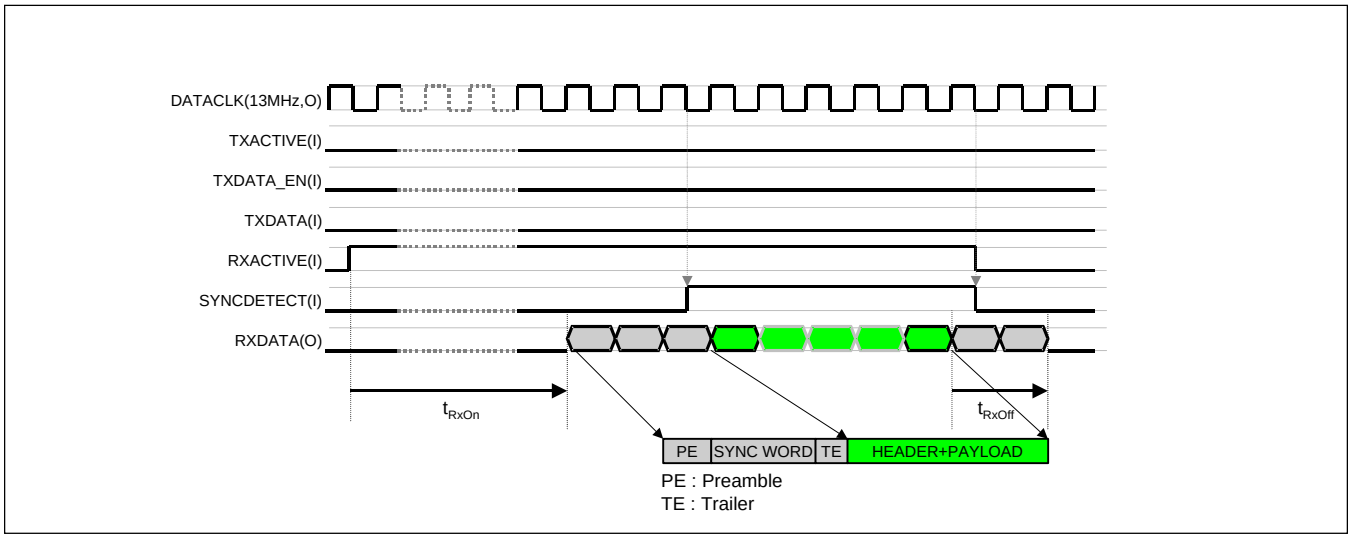


Figure 11. Receiver signal timing diagram in unidirectional interface



Receive operation in Bidirectional interface

Unlikely unidirectional interface, the primary procedure for data reception is to activate internal RXACTIVE signal by writing *HIGH* to RXA field of BT_RF_PLL_CTRL1 through DBUS interface. The RF circuitry starts to operate and send data after fixed time from writing data to the field. Right after writing *HIGH* to the field, the directional of bus is changed and PT8R1002 starts to drive TXDATA. Therefore, the baseband should disable the bus driving before the completion of register writing in order to prevent bus contention. Then, the baseband receives data and searches for the access code. During receive mode, DATACLK is sent from PT8R1002 to baseband as a timing reference. The PT8R1002 circuit sends the data to baseband at the rising edge of DATACLK, where the baseband latches the data at the falling edge of DATACLK. Prior to receiving information over air, the baseband transfers control information including the hop frequency over the DBUS interfaces, and enters PT8R1002 into ***search access code state*** after fixed time to turn on receiver circuitry by writing *HIGH* to RXA field of BT_RF_PLL_CTRL1. In the ***search access code state***, the baseband performs all of the tasks required to correlate with the access code from the receive data. When the baseband has correlated the access code, then it drives SYNCDETECT *HIGH* and makes PT8R1002 enter into ***receive payload state***. The bidirectional interface returns to the ***idle state*** by the baseband writing LOW to RXA field of BT_RF_PLL_CTRL1 to turn off RX circuitry after fixed T_{RxOff}. Right after writing LOW to the field, the directional of bus is changed and PT8R1002 disable to drive TXDATA. At that time, the baseband should enable the bus driving after the completion of register writing in order to prevent bus floating.

Power-up sequence

Figure 12. Receiver procedure timing-diagram in bidirectional interface

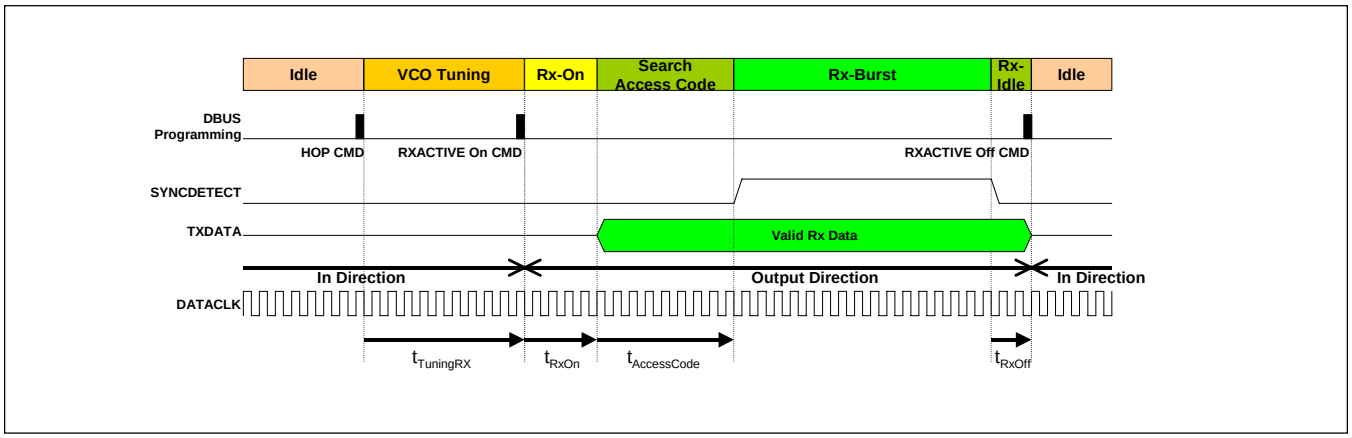
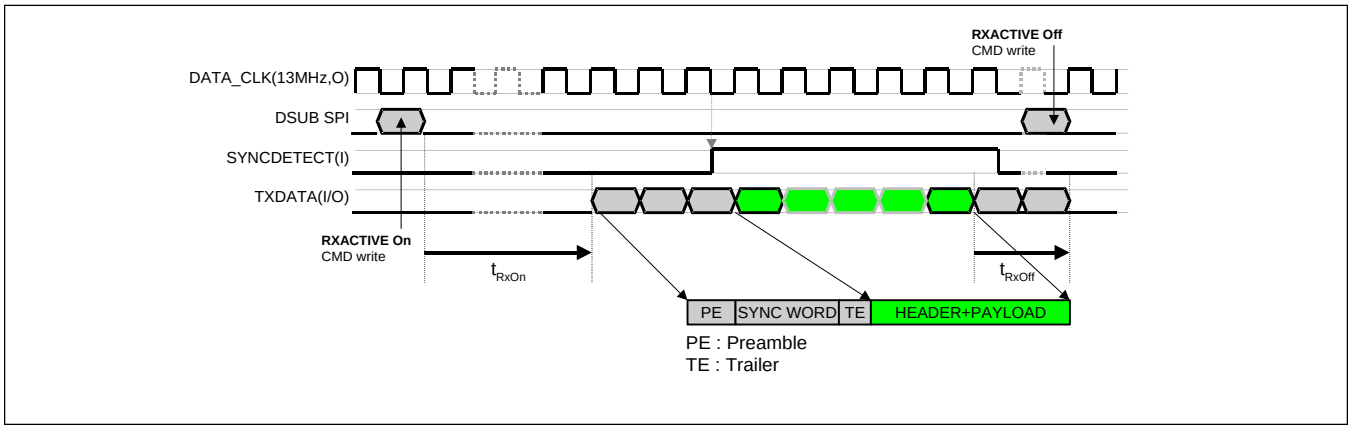
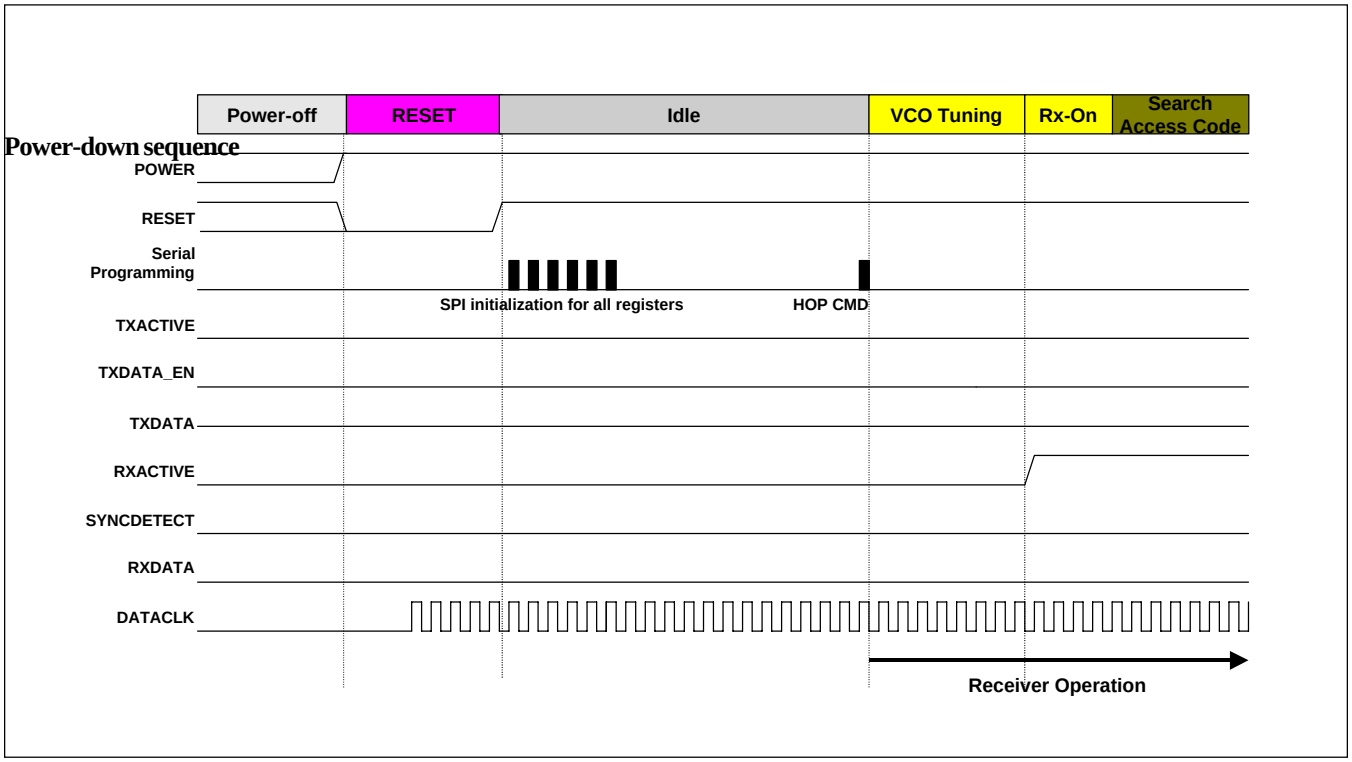


Figure 13. Receiver signal timing diagram in bidirectional interface



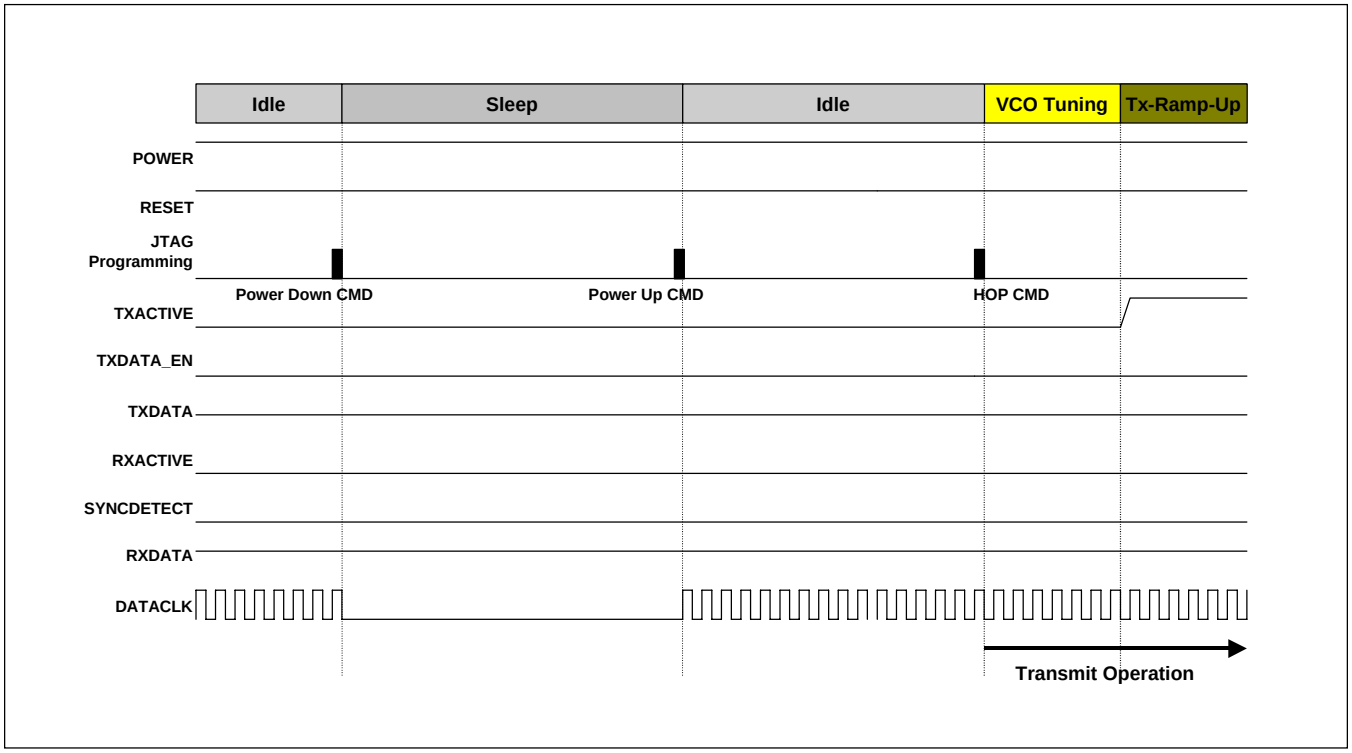
The power-up sequence of PT8R1002 is very simple mechanism. After power is applied to the PT8R1002, the activating RESET signal into LOW for t_{RESET} is the only required operation. After this procedure, PT8R1002 will come into idle mode for waiting transmit or receive operation indicated by Bluetooth baseband. Before this normal operation, all SPI register value should be initialized even though its value is set by the default value. The initialized value will be provided by PTI. After activating RESET signal, 13 or 16MHz baseband reference signal, DATACLK will be activated until execution of external power down command through SPI interface.

Figure 14. Power-up sequence procedure timing-diagram



The lowest operation power state of PT8R1002 is Sleep state, where all clocks including RF and baseband and circuits in the PT8R1002 is placed in their minimum power mode. In this mode, the control register can be accessed through serial interface logic and retain their programmed value. To enter into ***Sleep state***, power-down command which sets power-down of clock generator including crystal buffer should be programmed through the serial interface. After power-down command, the DATACLK from the PT8R1002 will stop until it comes back to ***Idle state***. To escape from ***Sleep state***, power-up command which sets power-up of clock generator should be programmed through the serial interface. After power-up command, the DATACLK will start again from the PT8R1002 into external baseband.

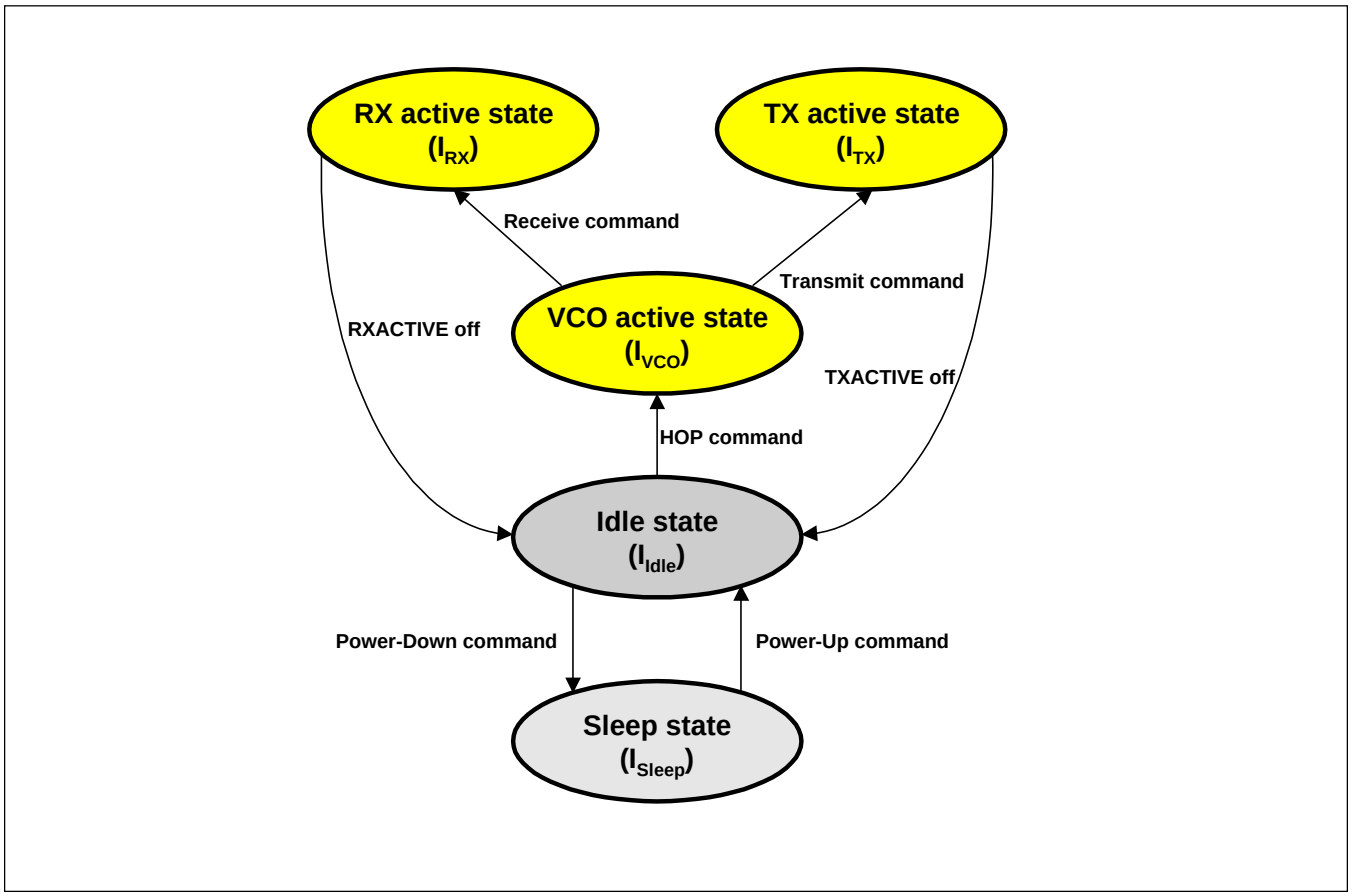
Figure 15. Power-down sequence procedure timing-diagram



Power control

In the PT8R1002, there are five different states with different current consumption; ***Sleep***, ***Idle***, ***VCO active***, ***TX active***, and ***RX active***. Upon reset, the PT8R1002 stays in the ***Idle state*** to wait for the command through serial programming interface from the baseband controller. In the Idle state, there is DATACLK from the radio to the baseband controller. In the ***Idle mode***, all RF circuits are shut down to reduce the static current consumption. Only the reference clock oscillator and DATACLK pump to the baseband is active. After HOP set command through the serial programming, the VCO will operate to lock the programmed channel frequency. Owing to the signal such as RXACTIVE or TXACTIVE, the PT8R1002 will enter into the active state such as ***TX active state*** and ***RX active state***. In those state, all RF circuits and GFSK modem will operate and result in the maximum current consumption. In the unidirectional mode, the falling signal of RXACTIVE or TXACTIVE will make the PT8R1002 into ***Idle state*** automatically. In the bidirectional mode, the explicit command to stop receive or transmission through serial programming will make the PT8R1002 into ***Idle state***. The PT8R1002 enters into ***Sleep state*** by power down command through serial programming. ***Sleep state*** is the least power consumption among other states and all clocks include reference oscillator will stop the operation as well as the power down of all RF circuits. In ***Sleep state***, only the serial programming interface logic can operate which uses clock from external device. However, the value of all registers will sustain until the wake up from ***Sleep state***. Following figure shows the state transition in terms of power control.

Figure 16. State transition diagram for power control



Timing parameter

Parameter	Min	Max	Comment
$t_{TuningTX}$, $t_{TuningRX}$	80usec	90usec	Time for PLL to lock to desired frequency
$t_{Ramp-Up}$	30usec	40usec	Time from TXACTIVE activating point to TXACTIVE_EN activating point **in unidirectional interface** Time from TXACTIVE on command writing point to SYNCDETECT activating point in **bidirectional interface**
$t_{Ramp-Down}$	3usec	5usec	Time from TXACTIVE_EN deactivating point to TXACTIVE activating point **in unidirectional interface** Time from SYNCDETECT deactivating point to TXACTIVE off command writing point **in bidirectional interface**
t_{RxOn}	110usec	130usec	Time from RXACTIVE activating point to received data sending point to the baseband **in unidirectional interface** Time from RXACTIVE on command writing point to received data sending point to the baseband **in bidirectional interface**
t_{RxOff}	3usec	5usec	Time from SYNCDETECT deactivating point to RX circuitry turn off point
t_{RESET}	100nsec	-	Time for minimum pulse width of RESET

Serial Programming Interface (JTAG interface)

The serial programming interface is a JTAG boundary-scan architecture compliant with IEEE 1149.1. Interconnection between the serial interface and external baseband consists of four 1-bit digital signals : control data input(TDI), control mode select (TMS), control clock (TCK) and control data output (TDO). You must refer to the full IEE std 1149.1-1990 Standard Test Access Port and Boundary-Scan Architecture document for a complete, definitive description of the operation of the fundamentals of the JTAG interface. PT8R1002 support TCK up to 13MHz.

Table 1. TAP instructions

Instruction	Opcode	Description
EXTEST	0x000000	EXTEST initiates testing of external circuitry, typically board-level interconnects and off chip circuitry. EXTEST connects the Boundary-Scan register between TDI and TDO in the SHIFT_DR state only. When EXTEXT is selected, all output signal pin values are driven by values shifted into the Boundary-Scan register and may change only on the falling-edge of TCK in the Update_DR state. Also, when EXTEST is selected, all system input pin states must be loaded into the Boundary-Scan register on the rising-edge of TCK in the Capture_DR state. Values shifted into input latches in the Boundary-Scan register are never used by the processor's internal logic.
SAMPLE / PRELOAD	0x000001	SAMPLE / PRELOAD performs two functions: • When the TAP controller is in the Capture-DR state, the SAMPLE instruction occurs on the rising edge of TCK and provides a snapshot of the component's normal operation without interfering with that normal operation. The instruction causes Boundary-Scan register cells associated with outputs to SAMPLE the value being driven by or to the processor. • When the TAP controller is in the Update-DR state, the PRELOAD instruction occurs on the falling edge of TCK. This instruction causes the transfer of data held in the Boundary-Scan cells to the slave register cells. Typically the slave-latched data is then applied to the system outputs by means of the EXTEST instruction.
IDCODE	0x011111	IDCODE is used in conjunction with the device identification register. It connects the identification register between TDI and TDO in the Shift_DR state. When selected, IDCODE parallel-loads the hard-wired identification code (32 bits) on TDO into the identification register on the rising edge of TCK in the Capture_DR state. NOTE: The device identification register is not altered by data being shifted in on TDI.
REGISTER PROGRAMMING	0x1SSSSS	REGISTER PROGRAMMING instruction select the REGISTER with address indicator SSSSS. • When the TAP controller is in the Capture-DR state, the REGISTER PROGRAMMING instruction occurs on the rising edge of TCK and executes a snapshot of register addressed SSSSS into serial register. • When the TAP controller is in the Update-DR state, the REGISTER PROGRAMMING instruction occurs on the falling edge of TCK. This instruction causes the transfer of data held in serial register to register addressed SSSSS.
BYPASS	0x111111	BYPASS instruction selects the Bypass register between TDI and TDO pins while in SHIFT_DR state, effectively bypassing the processor's test logic. 0 is captured in the CAPTURE_DR state. While this instruction is in effect, all other test data registers have no effect on the operation of the system. Test data registers with both test and system functionality perform their system functions when this instruction is selected.

SPI Registers Map

The values of all registers except read-only are set by default values after rest. The default values can be overrided by accessing each register. Typical register values are subject to change and should be obtained from PTI. During normal operation, SPI access should occur to address the following functions only.

- Programming PLL hop frequency of BT_RF_PLL_CTRL0
- Setting Tx power control value of BT_RF_TX_CTRL in the transmit mode
- Reading receive signal strength indication of BT_RSSI_STA in the receive mode
- Programming TXA or RXA of BT_RF_PLL_CTRL1 to indicate transmit or receive mode in bidirectional interface

Table 2. SPI register address map

Address	Name	Attribute	Description
0x00	BT_SOFT_RESET	write	RESET by serial interface*
0x01	BT_MODEM_CTRL	read/write	Modem control register
0x02	BT_RF_RX_CTRL	read/write	RF receiver control register
0x03	BT_RF_TX_CTRL	read/write	RF transmitter control register
0x04	BT_RF_BB_CTRL0	read/write	RF baseband control0 register
0x05	BT_RF_BB_CTRL1	read/write	RF baseband control1 register
0x06	BT_RF_PLL_CTRL0	read/write	RF PLL control0 register
0x07	BT_RF_PLL_CTRL1	read/write	RF PLL control1 register
0x08	BT_RF_PLL_CTRL2	read/write	RF PLL control2 register
0x09	BT_RF_PLL_CTRL3	read/write	RF PLL control3 register
0x0A	BT_RF_TIM_CTRL0	read/write	RF timing adjustment configuration0 register
0x0B	BT_RF_TIM_CTRL1	read/write	RF timing adjustment configuration1 register
0x0C	BT_RF_TIM_CTRL2	read/write	RF timing adjustment configuration2 register
0x0D	BT_RF_TIM_CTRL3	read/write	RF timing adjustment configuration3 register
0x0E	BT_RF_TIM_CTRL4	read/write	RF timing adjustment configuration4 register
0x0F	BT_RF_TIM_CTRL5	read/write	RF timing adjustment configuration5 register
0x10	BT_RF_AUX_CTRL0	read/write	RF auxiliary control0 register
0x11	BT_RF_AUX_CTRL1	read/write	RF auxiliary control1 register
0x12	BT_RSSI_STA	read	Modem RSSI register
0x13	BT_RF_STA	read	RF status register
0x14	BT_DAC_TEST_CTRL	read/write	DAC test register
0x15	BT_PWD_CTRL0	read/write	MODEM power detector register0
0x16	BT_PWD_CTRL1	read/write	MODEM power detector register1
0x17~0x1D	-	-	Reserved
0x1E	BT_PWDN	write	Power down register
0x1F	IDCODE	read	IDCODE

* Equivalent to hardware reset by asserting RESET pin.

* The values in all registers are the recommended initial value to be set by the serial programming interface, since some of them may be different value with the default configuration by hardware after reset. Also, these value can be changed in order to be optimized for special purpose. Please contact PTI semiconductor to get up-to-date configuration.

0x01	BT_MODEM_CTRL														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS														TEPM	
0	01011b					0111b				0	1	1	1	00b	

TEPM	External power amp drive enable mode 00 : off 01 : on 10/11 : on during TXACTIVE is high
CKS	Reference clock select flag 0 : 13MHz 1 : 16MHz

0x02	BT_RF_RX_CTL														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
01b		0	01b		1000b				0b	000000b					

0x03	BT_RF_TX_CTL														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			OS					TPG					TAG		
		1	0	0111b				11111b					001b		

OS	Output DATACLK PAD strength 0 : The driving capability of DATACLK is low 1 : The driving capability of DATACLK is high
TPG	External power amp gain control 00000b (1mA) ~ 11111b(0mA) with 32uA step
TAG	Transmission AGC gain control 000b(-3dB), 001b(-1.5dB), 010b(0dB), 011b(1.5dB), 100b(3dB), 101b(4.5dB), 110(6dB), 111(7.5dB)

0x04	BT_RF_BB_CTRL0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	1	1	0	1	11b		0	0011b				0

0x05	BT_RF_BB_CTRL1														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1010b				0	111b			011b			0000b			

0x06	BT_RF_PLL_CTRL0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXA	RXA	TG							CH						
0	0	0111111b							0000000b						

TXA	Internal TXACTIVE signal generation in bidirectional interface. Writing HIGH For more detail operation, refer to I/O description of transmit operation. This field does not affect in unidirectional interface.
RXA	Internal RXACTIVE signal generation in bidirectional interface. For more detail operation, refer to I/O description of receiver operation. This field does not affect in unidirectional interface.
TG[6]	Internal pre power amp gain control with bias change 1 : gain increase, 0 : gain decrease
TG[5:0]	Internal pre power amp gain control with driving ability 000000b(minimum gain) ~ 111111b(maximum gain)
CH	Frequency channel selection 0000000b : 0 channel(2402MHz), 0000001b : 1 channel(2403MHz), …

0x07	BT_RF_PLL_CTRL1														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	00000000								00000				

0x08	BT_RF_PLL_CTRL2														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	00b		11b		001b			00b		10b		1	010b		

0x09	BT_RF_PLL_CTRL3														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1000000000b										00b		00b		0	0

0x0A	BT_RF_TIM_CTRL0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBD				TBD				TBD				TBD			

0x0B	BT_RF_TIM_CTRL1														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBD				TBD				TBD				TBD			

0x0C	BT_RF_TIM_CTRL2														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBD				TBD				TBD				TBD			

0x0D	BT_RF_TIM_CTRL3														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBD				TBD				TBD				TBD			

0x0E	BT_RF_TIM_CTRL4														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBD				TBD				TBD				TBD			

0x0F	BT_RF_TIM_CTRL5														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBD		TBD		TBD		TBD		TBD		TBD		TBD			

0x10	BT_RF_AUX_CTRL0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	01b		0	1000b				1	1	000000b					

0x11	BT_RF_AUX_CTRL1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												PVN	PVL		
1	000b			01b		01b		1	0	0	0	0	100b		

PVN	Pre power amp output power detection enable 0 : disable 1 : enable
PVL	Pre power amp power detector reference level 000b(-7dBm), 001b(-5dBm), 010b(-3dBm), 011b(-1dBm) 100b(0dBm), 101b(1dBm), 110b(2dBm), 111b(3dBm)

0x12	BT_RSSI_STA															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PVO	RSSI_PO3						RSSI_RF				RSSI_AGC			

PVO	1 : The current power of pre power amp is more than PVL 0 : The current power of pre power amp is less than PVL
RSSI_AGC	AGC gain value with 3dB step from –3dB(0000b) to 42dB(1111b)

0x13	BT_POW_STA															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						CSS									

0x14	BT_DAC_TEST_CTRL															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			DE	DACI						DACQ					
			0	000000b						000000b					

0x15	BT_PWD_CTRL0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						PWD_START								AFS	DSS
						10000010b								1	1

0x16	BT_PWD_CTRL1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			PBD	PWR_TH3				PWR_TH2				PWR_TH1			
			0	1010b				0100b				0110b			

0x1E	BT_ PWDN															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															PD
															0

PD	1 : Power down mode enable 0 : Power down mode disable

0x1F	IDCODE															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IDCODE[31:16]															
0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

JTAG Registers Programming Timing Diagram in Unidirectional Interface

Figure 17. Serial register write programming timing diagram in JTAG

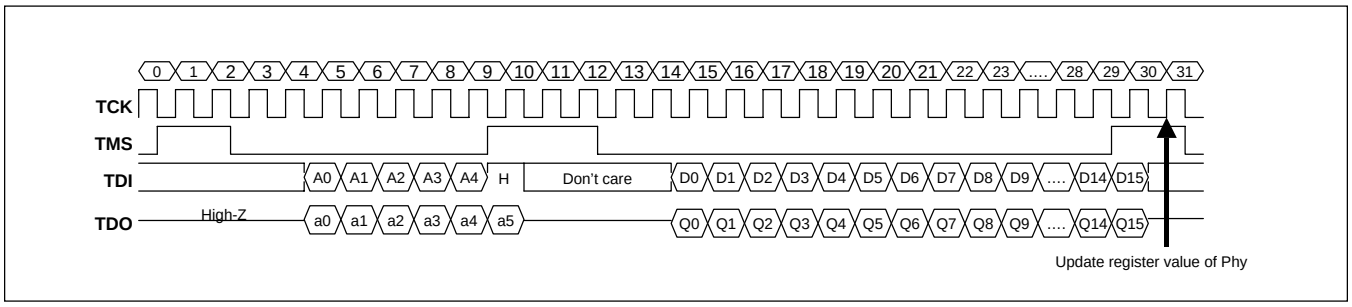
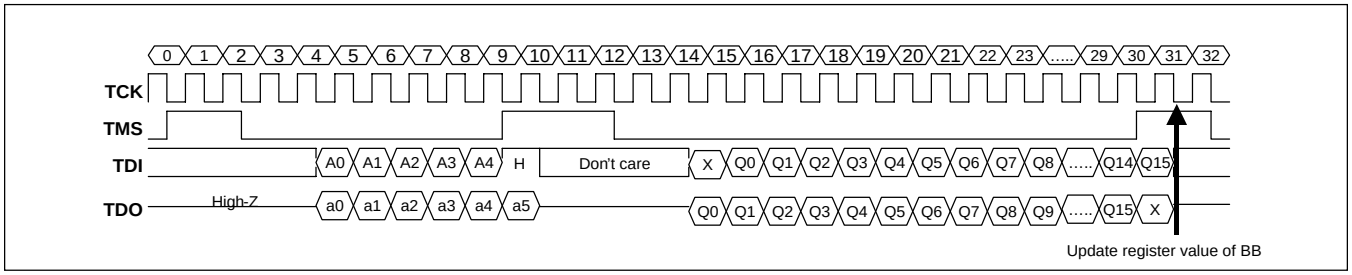


Figure 18. Serial register read programming timing diagram in JTAG



DBUS Registers Programming Timing Diagram in Bidirectional interface

Figure 19. Serial register write programming timing diagram in DBUS

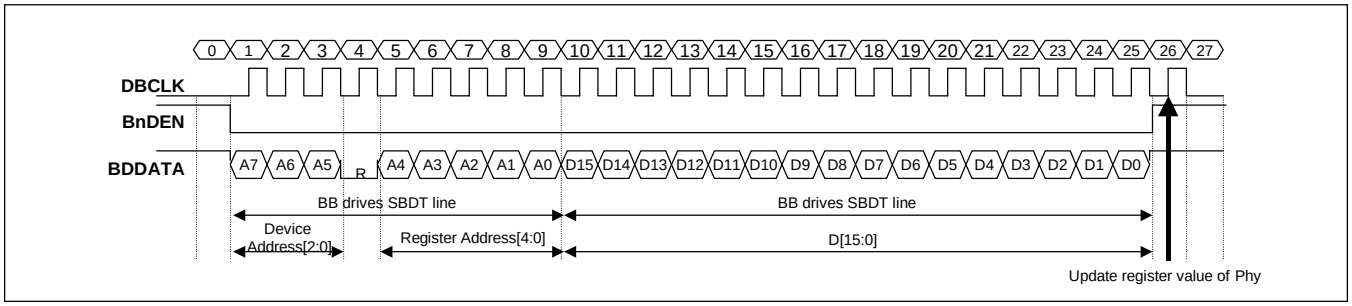
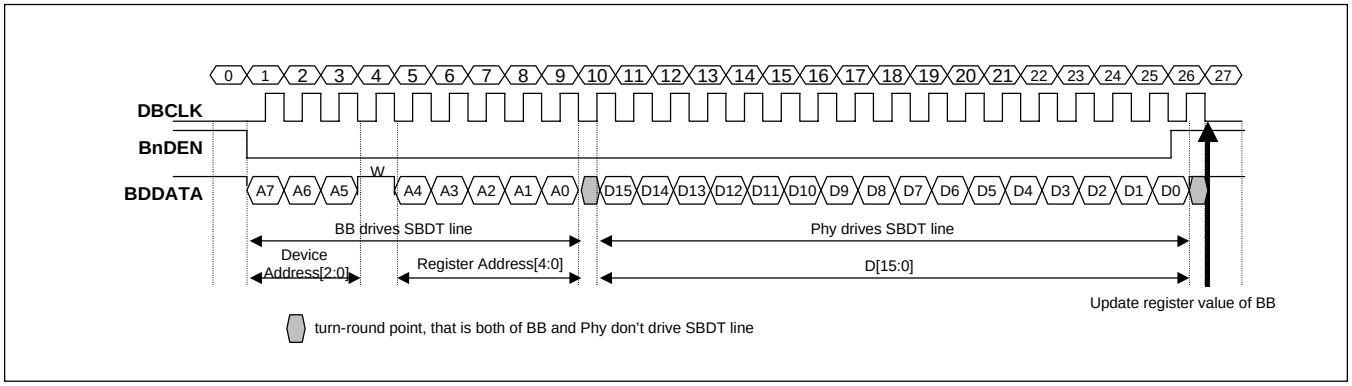


Figure 20. Serial register write programming timing diagram in DBUS



*A7, A6, A5 should be " 101" since it is allocated RF device address in BlueRF standard.

Electrical specifications

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent or latent damage to the device. These are absolute stress ratings only. Functional operation of the device is only implied at these or any other conditions in excess of those given in the operation sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Power Supply						
Supply Voltage All except IO_VCC (to GND)		V_{DD}	-0.5		5	V
Supply Voltage IO_VCC (to GND)		V_{PP}	-0.5		5	V
Input Voltage (All Input Pins)		V_I	-0.5		V_{DD}+0.5	V
Power						
Output Short Circuit Duration					CONT.	
Continuous Power Dissipation						
Temperature						
Operating Temperature Range			-40		85	°C
Storage Temperature Range		T_{STG}	-65		150	°C
Lead Temperature(Soldering, 10 sec)					300	°C

Recommended Operating Conditions

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Ambient Temperature	V_{DD} = 2.7V +/- 5%	T_A	-40	25	105	°C
Supply Voltage Except IO_VCC (To GND)	T_A= +25 C	V_{DD}		2.7		V
Supply Voltage IO_VCC (To GND)	T_A= +25 C	V_{PP}		3.3		V

DC Specifications

Unless otherwise noted, the specification applies for V_{DD} = 2.7V, T_A= +25 °C

Parameter	**Condition**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Digital Inputs						
Logical input High		V_{IH}	0.8V_{PP}		V_{PP}+0.3	V
Logical input Low		V_{IL}	-0.3		0.2V_{PP}	V
Input capacitance				3		pF
Input leakage current	0.5 < V_{IN} < V_{PP}-0.5	I_{LEAK}			5	μA
Digital Outputs						
Logical output High		V_{OH}	V_{PP}-0.4	V_{PP}		V
Logical output Low		V_{OL}		0	0.4	V
Output capacitance					10	pF
Current Consumption						
Sleep state		I_{SLEEP}		30		μA
Idle state		I_{IDLE}		2.1		mA
VCO active state		I_{VCO}		10		mA
TX active state		I_{TX}		40		mA
RX active state		I_{RX}		45		mA

Frequency Synthesizer Specifications

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Lock time	f_{CLK}=13MHz			80		μs
	f_{CLK}=16MHz			80		μs

Receiver Specifications

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Cascade Noise Figure	LNA + Mixer: max gain BB AGC: max gain			10		dB
	LNA + Mixer: max gain BB AGC: min gain			13		dB
	LNA + Mixer: min gain BB AGC: max gain			27		dB
	LNA + Mixer: min gain BB AGC: min gain			30		dB
Cascade Input 3rd Order Intercept Point	LNA + Mixer: max gain			-17		dBm
(@ LNA + Mixer output)	LNA + Mixer: min gain			1		dBm
Sensitivity	No frequency offset			-90		dBm
	±100KHz frequency offset			-88		dBm
Maximum receivable signal level	0.1% BER			2		dBm
C/I_{AWGN}	0.1% BER			18		dB
$C/I_{co\text{-}channel}$	0.1% BER			8		dB
$C/I_{@1MHz}$	0.1% BER			-6		dB
$C/I_{@2MHz}$	0.1% BER			-39		dB
$C/I_{\geq 3MHz}$	0.1% BER			-46		dB
Receiver turn-on time				20		μs

Transmitter Specifications

Parameter	**Condition**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Modulation index				0.32		
Maximum frequency deviation	Transmitting repetitive 00001111			160		kHz
Minimum frequency deviation	Transmitting repetitive 01			120		kHz
Transmit power				2		dBm
Power density at 500KHz offset	Maximum transmit power			25		dBc
Adjacent channel (@2MHz) power	Maximum transmit power			-47		dBm
Adjacent channel (≥3MHz) power	Maximum transmit power			-53		dBm
Transmitter turn-on time				8		μs

Application Note

Figure 20. Low cost digital data link using high speed MCU

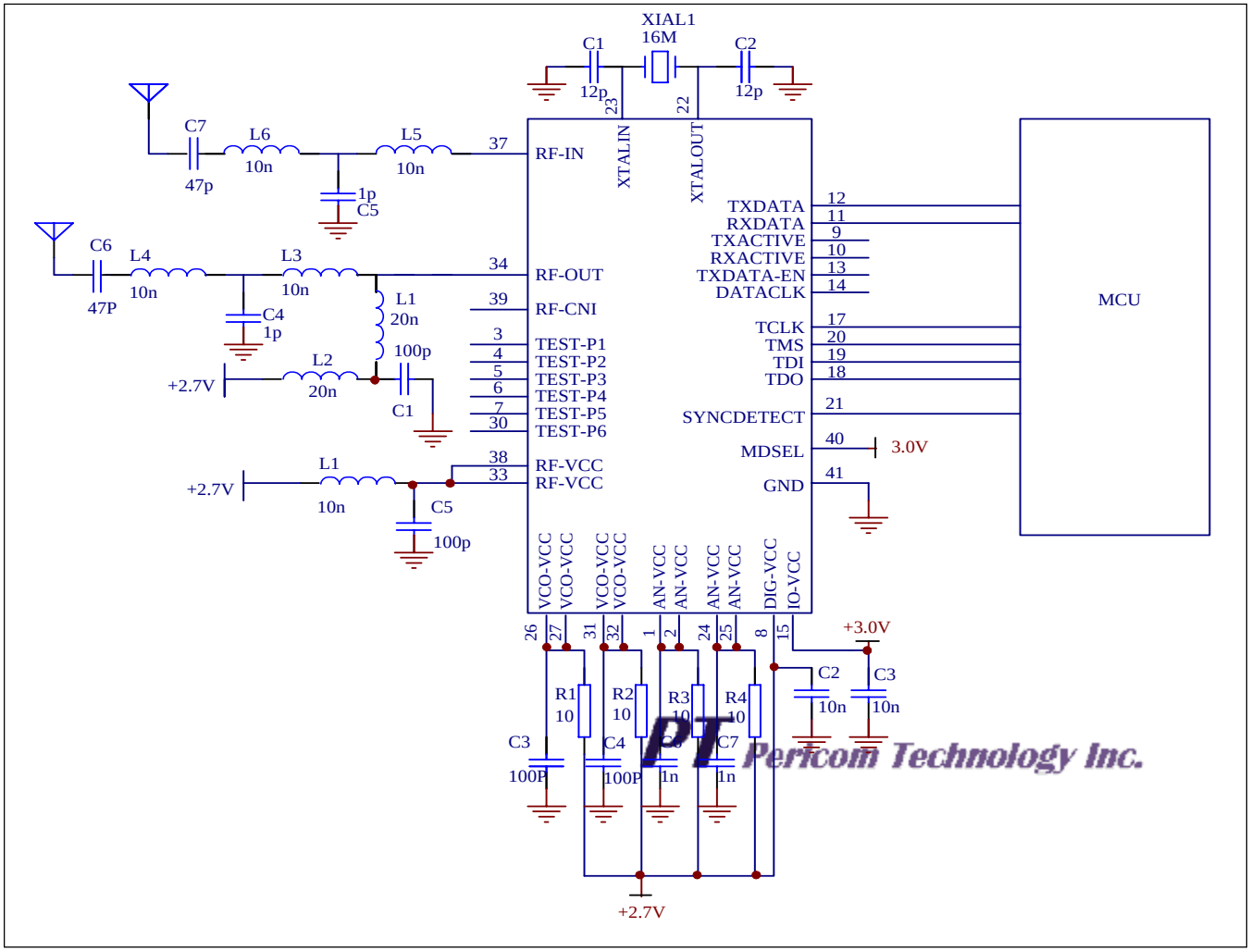
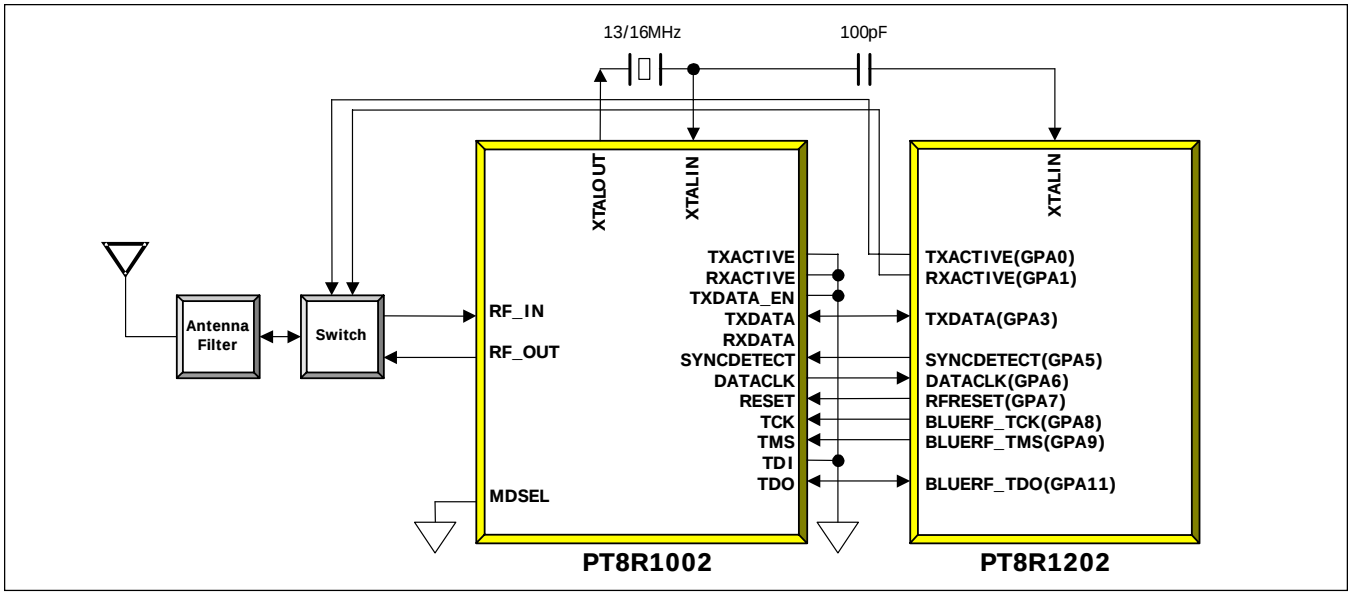
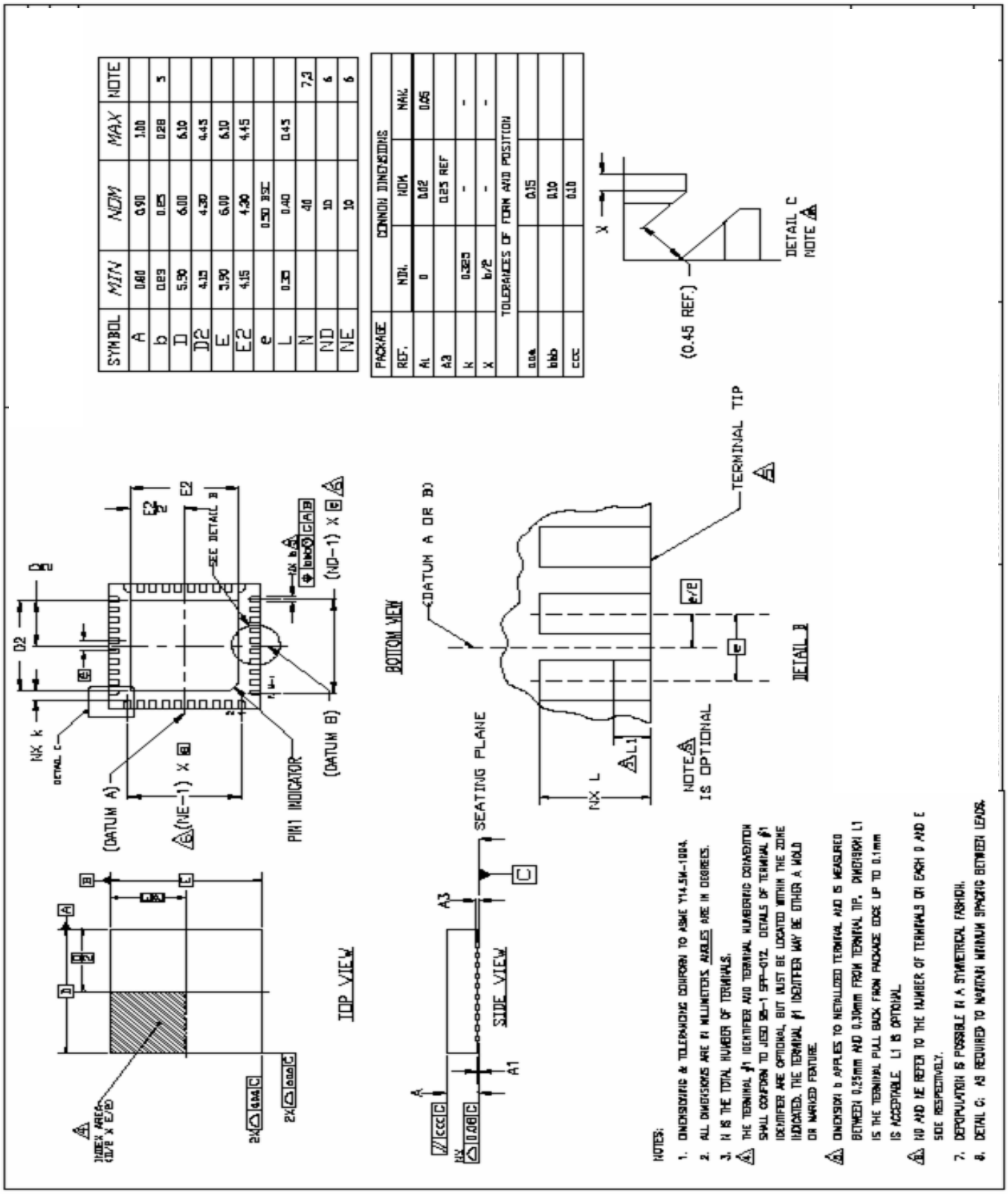


Figure 21. Bi-directional data link using Base Band Controller PT8R1202



Mechanical Information

Figure 22. 40-pin Quad Flat Non-lead Package



Notes

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